NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. M4065.0223/P223
Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

and invented by:

Chih-Chen Cho

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 19 pages(s) and including the following:
   - a. [X] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [X] Background of the invention
   - f. [X] Brief summary of the invention
   - g. [X] Brief description of the drawings *(if drawings filed)*
   - h. [X] Detailed description
   - i. [X] Claims as classified below
   - j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal [X] Informal Number of sheets: 5

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	38	- 20 =	18	x $18.00	$324.00
Independent Claims	5	- 3 =	2	x $78.00	$156.00
Multiple Dependent Claims (check if applicable) ☐					
Other Fees (specify purpose): Assignment Recordation Fee					$40.00
				BASIC FEE	$690.00
				TOTAL FILING FEE	$1,210.00

☒ A check in the amount of $1,210.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: March 2, 2000

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Docket No.: M4065.0223/P223
Micron No.: 99-0506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

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BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

FIELD OF THE INVENTION

The present invention relates to the fabrication of semiconductor devices. More particularly, the present invention relates to the backend metallization process used in the formation of semiconductor devices.

BACKGROUND OF THE INVENTION

There are a variety of semiconductor device types, one particular semiconductor device being a semiconductor memory device, such as random access memory (RAM) device. Known types of RAM devices include static random access memory (SRAM) devices and dynamic random access memory (DRAM) devices. A DRAM device contains an array of individual memory cells. Each cell includes an integrated circuit on a substrate and conductive material for electrically connecting the cell to other structures of a memory circuit.

With reference to FIG. 1, one conventional method for depositing conductive material for backend metallization, is a single Damascene method. FIG. 1 shows a simplified single Damascene method for forming a metallization connection to a substrate. It includes depositing a non-conductive layer of material 20, e.g. borophosphosilicate glass (BPSG), on a substrate 24 and pattern etching an opening within the material 20. A conductor, e.g. a metal or a doped polysilicon, is deposited over the material 20, thereby filling in the opening and providing a covering layer on the material 20. Chemical-mechanical polishing of the conductor removes the layer of

conductor on the material 20, leaving a conductive plug M_1. The conductive plug M_1 is positioned on a doped region 22 provided in the substrate 24. An additional layer of non-conducting material 20, e.g. BPSG, is then deposited over the conductive plug M_1 and the previously deposited material 20. A via 21 is then etched in the material 20 above the conductive plug M_1. A conductive barrier material 12 is then deposited within the via 21 and over the additional material 20. Then another conductive layer 16 is deposited over the barrier layer 12, thereby completing an electrical connection between conductive layer 16 and doped region 20.

Vias 21 may be formed with a positive overlap (the conductive plug M_1 is of a greater diameter than the via 21), a zero overlap (the conductive plug M_1 and the via 21 are the same diameter), or a negative overlap (the conductive plug M_1 has a smaller diameter than the via 21). In FIG. 1, a negative overlap is shown. Because of the decreasing sizes of semiconductor devices, zero overlaps and negative overlaps are becoming more prevalent.

The conductive layers 12, 16 may be formed of any suitable conductive material, such as aluminum, copper or a highly doped polysilicon. The material 20 is preferably formed of a non-conductive material which is relatively easily removed in a chemical-mechanical polishing or etching process. Most preferably, and as noted, the material 20 is a doped silicate glass, such as, for example, BPSG.

In addition to the single Damascene method described above, a double Damascene method may be used to form a conductive connection. A double Damascene method for forming trench capacitors is described in "Dual-Damascene Challenges Dielectric Etch," Semiconductor International, p. 68-72, August 1999.

One disadvantage associated with the above-described fabrication method is that sometimes the etched via 21 in the material 20 is offset slightly relative to the plug M_1, as shown in FIG. 2. This most usually occurs in zero overlap and/or negative overlap fabrication processes. The etching of such an offset via 21 creates an offset opening portion 25 along the side of the conductive plug M_1, which during the subsequent layering of the conductive layers 12, 16 may form an air gap 26 (FIG. 2). Initially, the air gap 26 is relatively small, but as the conductive layers are deposited at elevated temperatures, the gas trapped in the gap 26 expands. The presence of a sizable and expanding air gap 26 sometimes prevents deposition of, or causes a rupture in, a continuous conductive layer 12 within the opening 25, which in turn may cause a defect in the conductive connection 14. This is because the conductive layer 12 is typically formed by first depositing a seeding layer for subsequent conductor formation. When part of the seeding layer is missing, a void is formed in both the seeding layer and the conductor which is formed above it. Further, the lack of a continuous conductive layer 12 may create a higher resistance in the ultimately formed conductive connection 14.

One approach at alleviating this disadvantage is to utilize a different conductive material for the conductive layer 12. Whereas aluminum or copper generally have been used for the conductive layer 12 (FIG. 2), titanium, titanium nitride or tungsten may be used in a conductive layer 112 of a conductive connection 114 (FIG. 3) of a semiconductor device 100. While the use of such materials tends to pinch off the size of an air gap 126 formed in an offset opening 125, in instances where the offset is relatively large, the conductive layer 112 still may not be formed as desired, thus creating the problems noted above. Further, titanium, titanium nitride and

tungsten all have a higher electrical resistance than aluminum and copper within the ultimately formed conductive connection, which may create other problems.

There thus exists a need for a fabricated semiconductor device which does not tend to form the offset gap shown in FIG. 2.

SUMMARY OF THE INVENTION

The present invention avoids the offset gap shown in FIG. 2 by preventing any part of the via 21 from being etched along side of the plug M_1. This is accomplished by fabricating a structure in which a conductive connector comprises a conductive plug positioned within an insulator and provided on a substrate connection region, an etch-stop layer deposited on the insulator and around the conductive plug, an intermediate non-conductive layer having an etched via over the plug, a first conductive layer deposited in and in contact with the etched via and having a portion in contact with the conductive plug, and a second conductive layer deposited over the first conductive layer. The etch step layer prevents the via from being etched along the side of the plug during via formation.

According to another aspect of the present invention, a memory device including at least one memory cell may be provided with the just described conductive connector.

The present invention also relates to a method of making a semiconductor conductive connector. The method includes providing a first layer of dielectric material on an integrated circuit substrate, forming a conductive plug within the first dielectric material, providing an etch-stop layer over the first dielectric layer and around

the conductive plug, providing a second layer of dielectric material over the conductive plug and etch-stop layer, etching the second layer of dielectric material to the conductive plug and etch-stop layer to form a via, and forming a conductive connector in the via in contact with the conductive plug.

These and other advantages and features of the invention will be more readily understood from the following detailed description which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an idealized cross-sectional view of a conventionally fabricated conductor connection in a semiconductor device.

FIG. 2 is a cross-sectional view like FIG. 1 showing an offset via.

FIG. 3 is a cross-sectional view like FIG. 2 showing another offset via.

FIG. 4 is a cross-sectional view of a semiconductor device constructed in accordance with an embodiment of the present invention.

FIG. 5 is a cross-sectional view of a semiconductor device constructed in accordance with another embodiment of the present invention.

FIG. 6 illustrates a method of making the device shown in FIG. 5.

FIG. 7 illustrates a method of making semiconductor products in accordance with an embodiment of the present invention.

FIG. 8 illustrates a processor-based system constructed in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring now to the drawings, where like numerals designate like elements, there is shown in FIG. 4 a semiconductor device 200 with a substrate 24 and a conductive connection 214 that may be formed by either the single Damascene or double Damascene methods. The substrate 24 can be made of any material typically used as a substrate in integrated circuit fabrication. The conductive connection 214 includes the first and second conductive layers 12, 16. The conductive layers 12, 16 may be formed of one or more of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten. The semiconductor device 200 includes the material 20 surrounding the via 21. The metal plug M_1 is embedded within a first insulator layer 230, for example, a BPSG layer, and a hard mask layer 228. The hard mask layer 228 may be formed of any material capable of withstanding the subsequent etching process described below, such as, for example, silicon nitride, silicon carbide, silicon dioxide, or BLOK® (a mixture of silicon nitride and silicon carbide).

If the hard mask 228 is formed of, for example, silicon nitride, a plasma etch using CF_4 or C_2F_6 as the etching gas may be utilized to form the via 21. When either of these etching gases reacts with the BPSG material 20, the oxygen contained within the material 20 is released and will react with the carbon in the etching gas to form carbon dioxide and desorb. However, when the etching gas reacts with the silicon nitride, there is no oxygen in the film, so a polymer containing carbon is formed. The

polymer slows down or stops the etch of the silicon nitride, particularly, when the carbon to flourine ratio is high.

The result of this etching process is that etching of the insulating layer 20 to form the via 21 will stop at the hard mask 228 and the formation of an offset opening like the offset openings 25, 125 shown in FIGS. 2 and 3 will be prevented. Accordingly, as shown in FIG. 4, the via 21 etching stops at the top surface of the conductive plug M_1 and mask 228. The layers 12, 16 can then be fabricated in the via 21 and the conductive connection 214 can be used to connect the doped region 22 to other portions of the partially illustrated semiconductor device 200.

Next, a method of forming the conductive connection 214 (FIG. 4) will be described with reference to FIG. 7. At step 400, the insulator layer 230 and the hard mask 228 are deposited on the substrate 24 containing the doped region 22. The doped region 22 may be formed by way of an ion implant. Further, the doped region 22 may serve as an active region in a memory cell, such as cell 513 (described below). It should be noted that the doped region 22 is merely illustrative of just one point on a substrate where an electrical connection is needed. The conductive connection 214 can be fabricated wherever a conductive path is needed. An opening is formed in the insulator 230 and the hard mask 228 layers at step 405. The opening is preferably formed through the use of a photoresist and masking, followed by one or more anisotropic etching steps. The opening alternatively may be formed through mechanical or laser drilling. After stripping the photoresist, conductive material, e.g., polysilicon, is deposited over the insulator 230, including in the opening, and is chemical-mechanical polished (CMP) to form the conductive plug M_1 at step 410.

The planarizing process causes the top surface of the etch-resistant layer 228 to be co-planar with the top surface of the conductive element M_1.

An insulating layer 20, e.g. BPSG, is then deposited on the insulator 230 (step 415) and the via 21 is subsequently etched into the insulating layer 20 (step 420). The etching of via 21 is preferably accomplished by laying a photoresist over the material 20, exposing and developing the phtotoresist to mask a portion of the material 20 that is not to be etched, and then etching the via 21 in the unmasked region. As noted, the hard mask 228 is formed of a material which is relatively resistant to the etching chemistry, and hence acts as an etch stop so there is little or no etching below the top level of the conductive plug M_1. The first conductive layer 12 is then deposited at step 425 and the second conductive layer 16 is deposited on the first conductive layer 12 at step 430, thereby creating the conductive connection 214.

FIG. 5 shows a multi-step semiconductor device 300 having a conductive connection 314. The multi-step semiconductor device 300 has a greater conductive surface area which can be used to form container capacitors, useful, for example, in a memory device. A via 121 is etched above the metallic plug M_1 in several steps to create via portions 122 and 123. The via portion 123 has a greater diameter than the via portion 122, allowing the deposition of more area of first and second conductive layers 112 and 116. If capacitors are formed in the FIG. 5 via portions 122 and 123, then the conductive layer 112 is replaced by a three layer structure formed of a conductor layer, a dielectric layer, and another conductive layer, as is known in the art.

Referring now to FIGS. 6 and 7, to form the semiconductor device 300 (FIG. 5), the via 121 is etched in several steps to form the via portions 122 and 123.

Specifically, a layer of the material 120 is deposited over the hard mask 228 and the plug M_1 (step 410). After laying down a photoresist 130 and a mask 132, photoresist 130 is partially developed, and the developed portions and the mask 132 are removed and the remaining photoresist 130 is stripped. The via portion 122 is then etched at step 415. A second layer of photoresist 130 is then deposited. A second mask 134 is utilized to develop a portion of the second photoresist layer 130. The developed portion is removed as described above. Further the mask 134 is removed and the remaining photoresist 130 is stripped. The via portion 123 is then etched at step 435. After the via portions 122, 123 have been formed, and the photoresist 130 and mask 134 have been removed, layers 112, 116 (which are similar to the layers 12, 16, respectively) are deposited in the via 121 (steps 425, 430).

Referring now to FIG. 8, a device constructed in accordance with the invention can be used in a memory circuit, such as a DRAM device 512, or other electronic integrated circuit, within a processor-based system 500. The processor-based system 500 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 500 includes a central processing unit (CPU) 502, which may be a microprocessor. The CPU 502 communicates with the DRAM device 512, which has cells 513 that include the semiconductor device 200 (or the semiconductor device 300), over a bus 516. The CPU 502 further communicates with one or more I/O devices 508, 510 over the bus 516. Although illustrated as a single bus, the bus 516 may be a series of buses and bridges commonly used in a processor-based system. Further components of the system 500 may include a read only memory (ROM) device 514 and peripheral devices

such as a floppy disk drive 504, and CD-ROM drive 506. The floppy disk drive 504 and CD-ROM drive 506 communicate with the CPU 502 over the bus 516.

The present invention provides a semiconductor device which does not suffer from the aforementioned disadvantages caused by an etched area to the side of the conductive plug M_1. The present invention further provides a method for making semiconductor devices without forming air gaps in trenches offset from a conductive plug.

While the invention has been described in detail in connection with preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor structure comprising:

an insulator layer;

a conductive plug positioned within said insulator layer;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having an etched via at least partially over said conductive plug; and

a conductive connector formed in said via in electrical contact with said plug.

2. The semiconductor structure of claim 1, wherein said conductive connector comprises:

a first conductive layer deposited in and in contact with said etched via, said first conductive layer including a portion in contact with said conductive plug; and

a second conductive layer deposited over said first conductive layer.

3. The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon nitride.

4. The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon carbide.

5. The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon dioxide.

6. The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon nitride and silicon carbide.

7. The semiconductor structure of claim 1, wherein said non-conductive layer comprises doped silicate glass.

8. The semiconductor structure of claim 7, wherein said doped silicate glass comprises borophosphosilicate glass.

9. The semiconductor structure of claim 2, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

10. The semiconductor structure of claim 1, further comprising a substrate with a connection region, wherein said conductive plug is provided over said connection region.

11. A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug positioned within an insulator layer and provided on said active region, said conductive plug being in contact with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having an etched via over said plug; and

at least one conductive layer in said via in electrical connection with said plug.

12. The semiconductor memory device of claim 11, wherein said at least one conductive layer comprises:

a first conductive layer formed in said etched via, said first conductive layer including a portion in contact with said conductive plug; and

a second conductive layer deposited over and in contact with said first conductive layer.

13. The semiconductor memory device of claim 11, wherein said intermediate layer comprises doped silicate glass.

14. The semiconductor memory device of claim 13, wherein said doped silicate glass comprises borophosphosilicate glass.

15. The semiconductor memory device of claim 12, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

16. The semiconductor memory device of claim 12, wherein said second conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, titanium, titanium nitride and tungsten.

17. The semiconductor memory device of claim 11, further comprising an array of said memory cells.

18. A semiconductor device comprising:

a conductive element;

an etch-resistant layer surrounding an upper portion of said conductive element;

a non-conductive layer over said etch resistant layer and having a via over said conductive element, said via extending down to a level of said conductive element and etch resistant layer; and

a conductive material located in said via, wherein said conductive material contacts said conductive element.

19. The semiconductor device of claim 18, further comprising a doped region connected to said conductive element.

20. The semiconductor device of claim 18, wherein said non-conductive layer comprises doped silicate glass.

21. The semiconductor device of claim 20, wherein said doped silicate glass comprises borophosphosilicate glass.

22. The semiconductor device of claim 18, wherein said conductive material comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

23. The semiconductor device of claim 18, further comprising a conductive layer located in said via.

24. The semiconductor device of claim 18, further comprising a connection region, wherein said conductive material is located over said connection region.

25. A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a substrate supporting a connection region;

a conductive plug positioned within an insulator and provided on said connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having an etched via over said conductive plug; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said etched via, said first conductive layer including a portion in contact with said conductive plug.

26. The processor-based system of claim 25, wherein said conducting connector further comprises a second conductive layer deposited over said first conductive layer, a semiconductor die being electrically connected to said conductive connector.

27. The processor-based system of claim 26, wherein said connection region comprises a doped region within said substrate.

28. The processor-based system of claim 26, wherein said intermediate layer comprises doped silicate glass.

29. The processor-based system of claim 28, wherein said doped silicate glass comprises borophosphosilicate glass.

30. The processor-based system of claim 26, wherein said first conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

31. The processor-based system of claim 26, wherein said second conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

32. The processor-based system of claim 26, further comprising a substrate, and wherein said connection region is located in said substrate, and wherein said conductive plug is located over said connection region.

33. A method of making a semiconductor device, said method comprising:

forming a layer of insulating material over a substrate;

forming a conductive plug within said first layer of insulating material;

forming an etch-stop layer over said first layer of insulating material and around said conductive plug;

forming a second layer of insulating material over said conductive plug and etch-stop layer;

etching said second layer of insulating material to said conductive plug and etch-stop layer to form a via.

34. The method of claim 33, further comprising depositing at least a first conductive layer in said via.

35. The method of claim 34, comprising depositing a second conductive layer over said first conductive layer in said via.

36. The method of claim 33, wherein said plug is formed by:

forming an opening in said first layer of insulating material;

depositing a conductive material on said first layer of insulating material, filling said opening; and

abrading said conductive material from the top surface of said first layer of insulating such that only conductive material within said opening remains.

37. The method of claim 36, wherein said abrading comprises chemical-mechanical polishing of said conductive material.

38. The method of claim 36, wherein said conductive plug is connected to a doped region in said substrate.

ABSTRACT

A semiconductor device and a method of making it are described. During the formation of the semiconductor device, a hard mask is formed of an etch-resistant material. The mask prevents etchant from etching an area within a dielectric material near a conductive plug. The mask may be formed of a nitride. Conductive material is then deposited withinan etched via and is contacted with the conductive plug.

FIG. 1

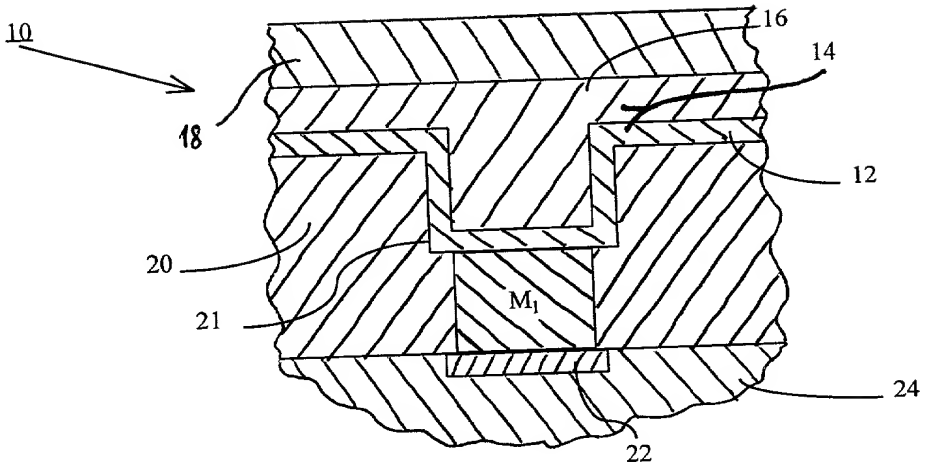


FIG. 2

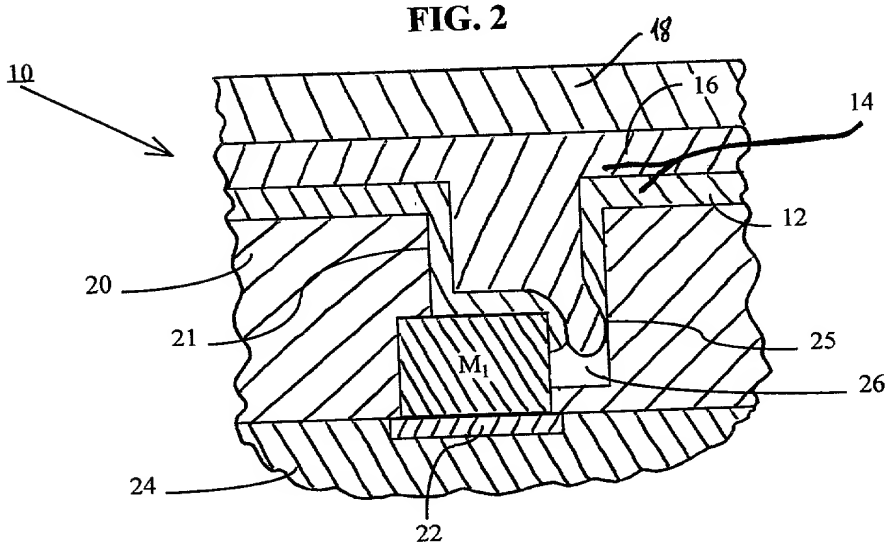
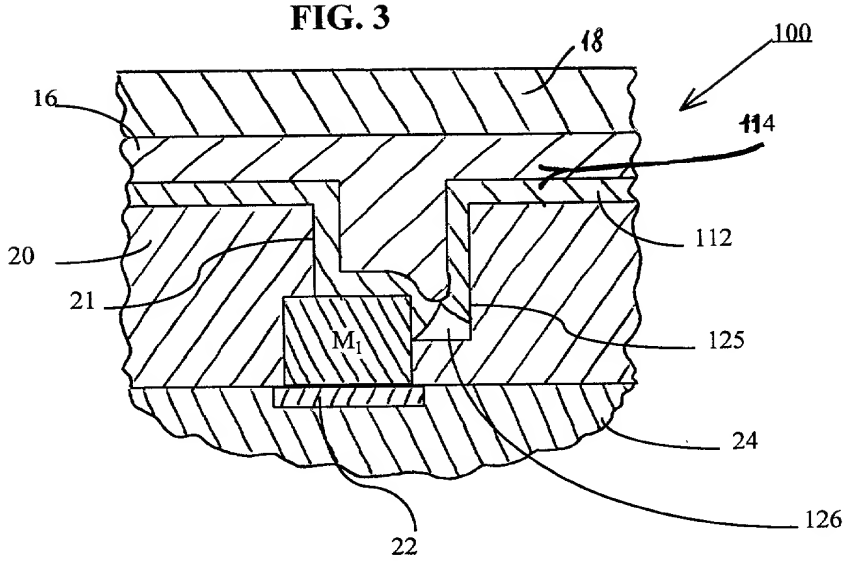


FIG. 3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16
114
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M_1
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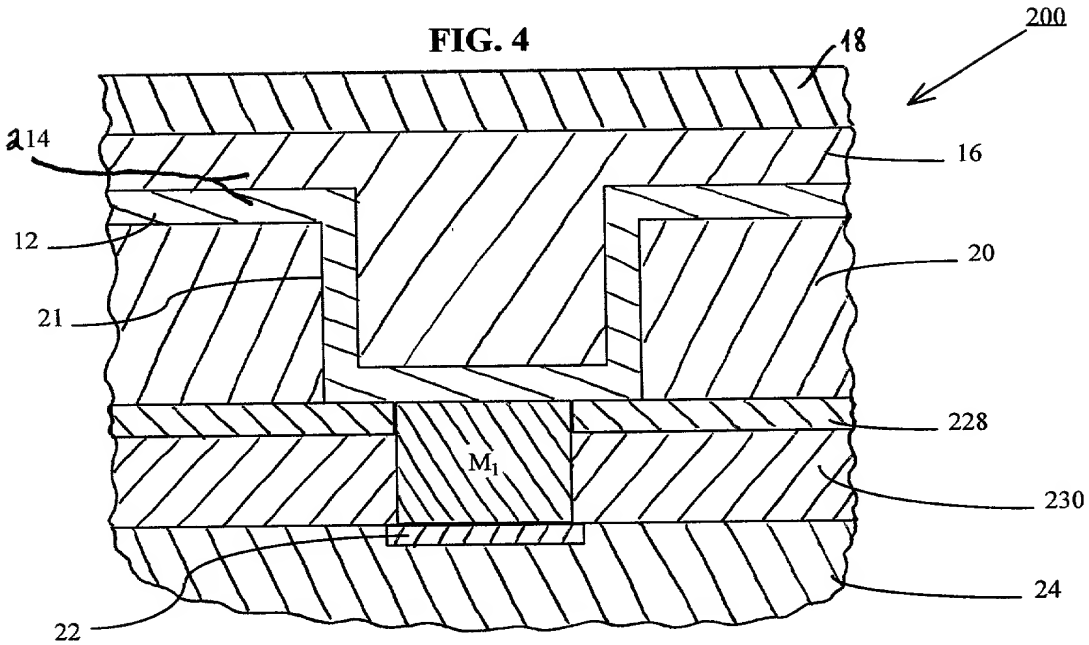
126
22

FIG. 4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214
16
12
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21
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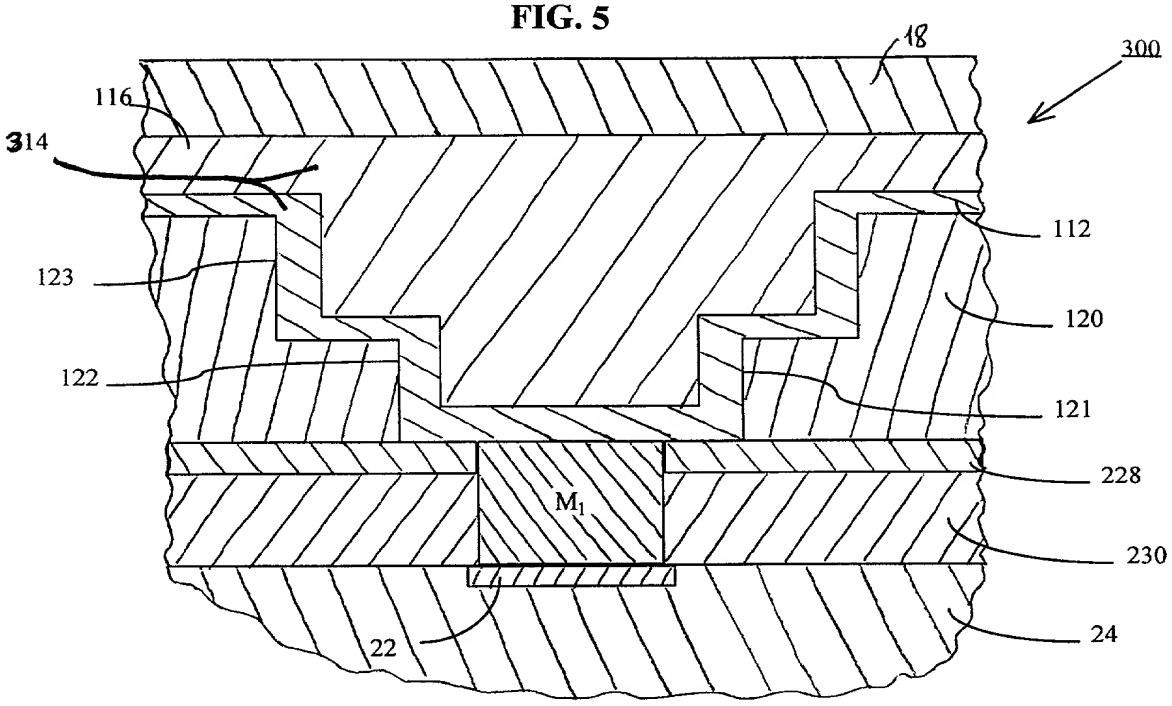
M_1
230
24
22

FIG. 5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300
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123
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M_1
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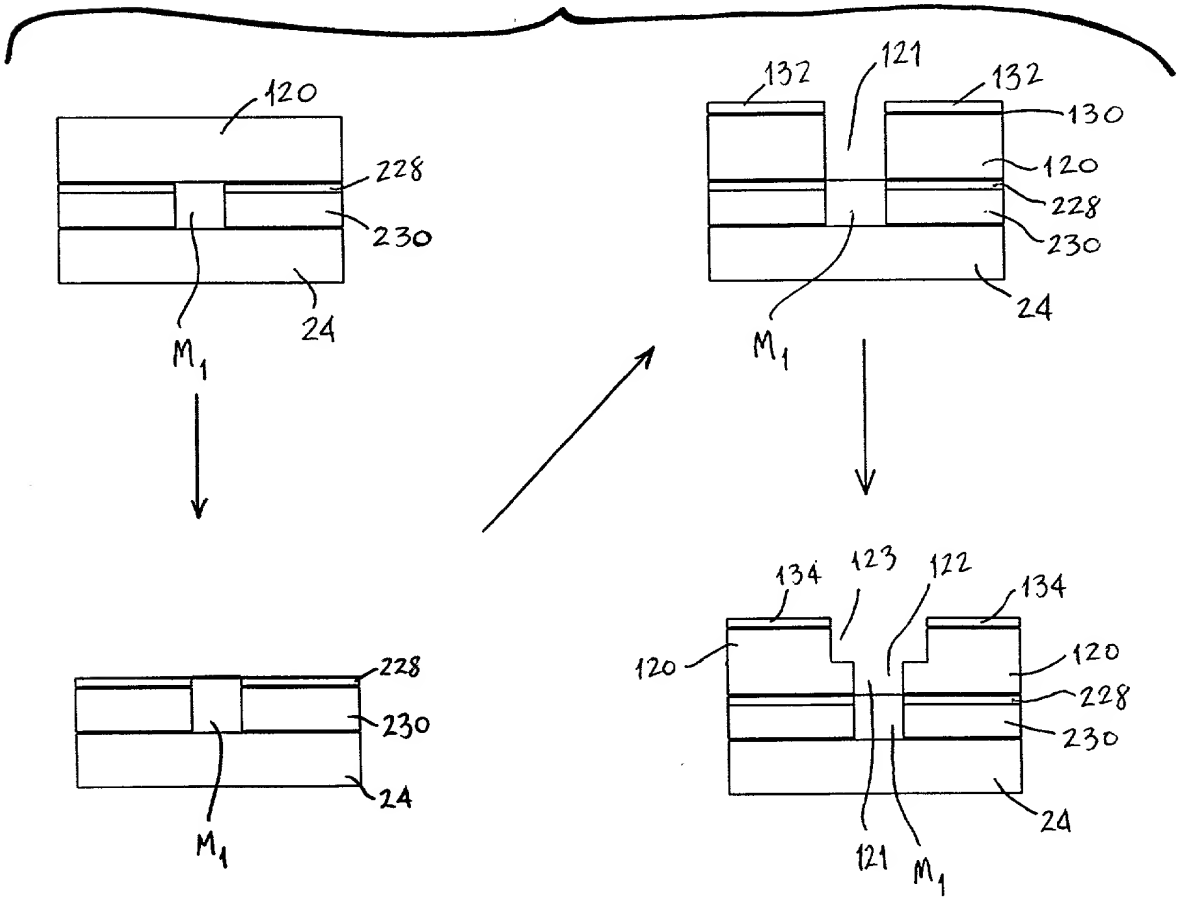
FIG. 6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230
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M_1

FIG. 7

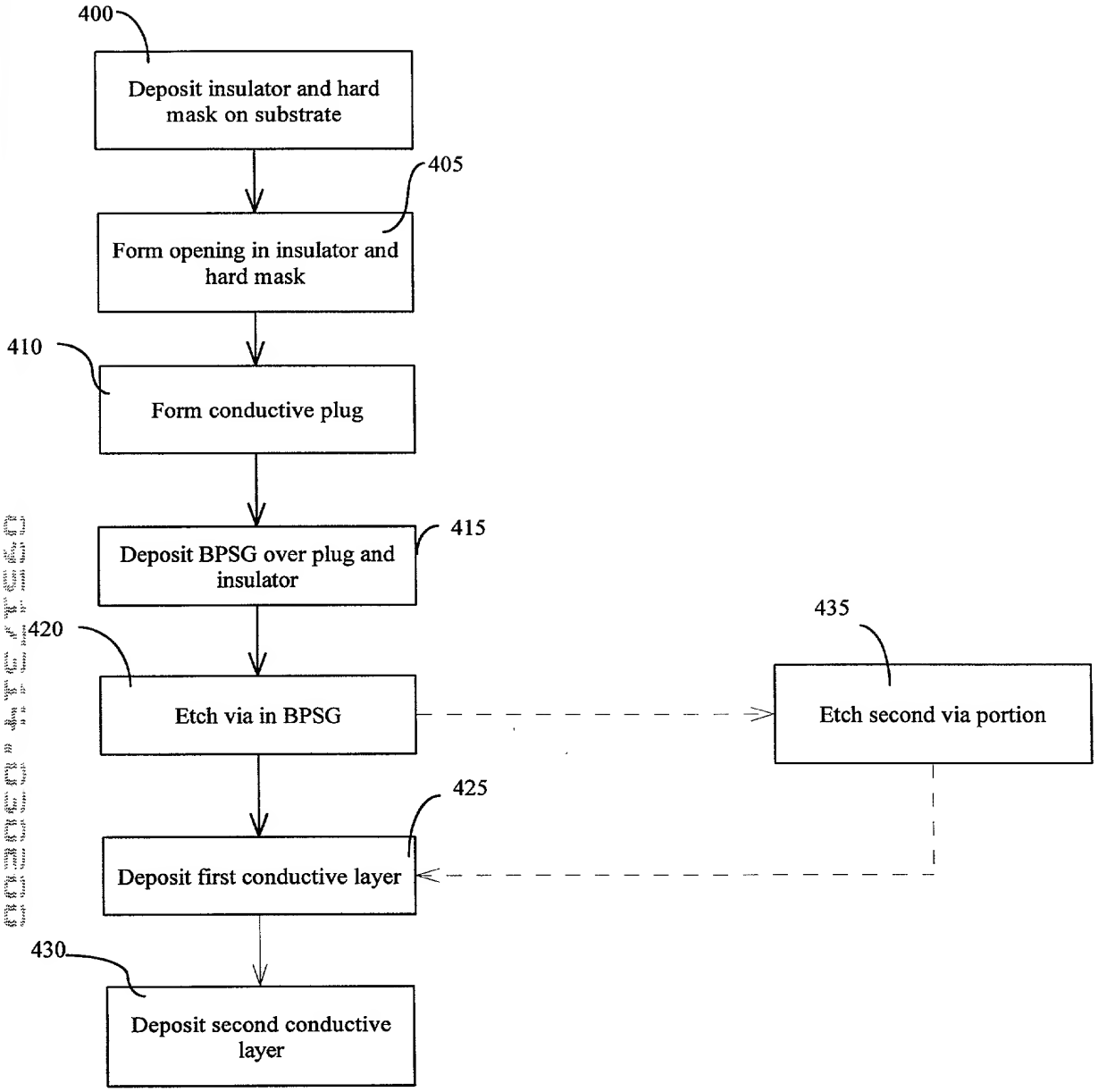
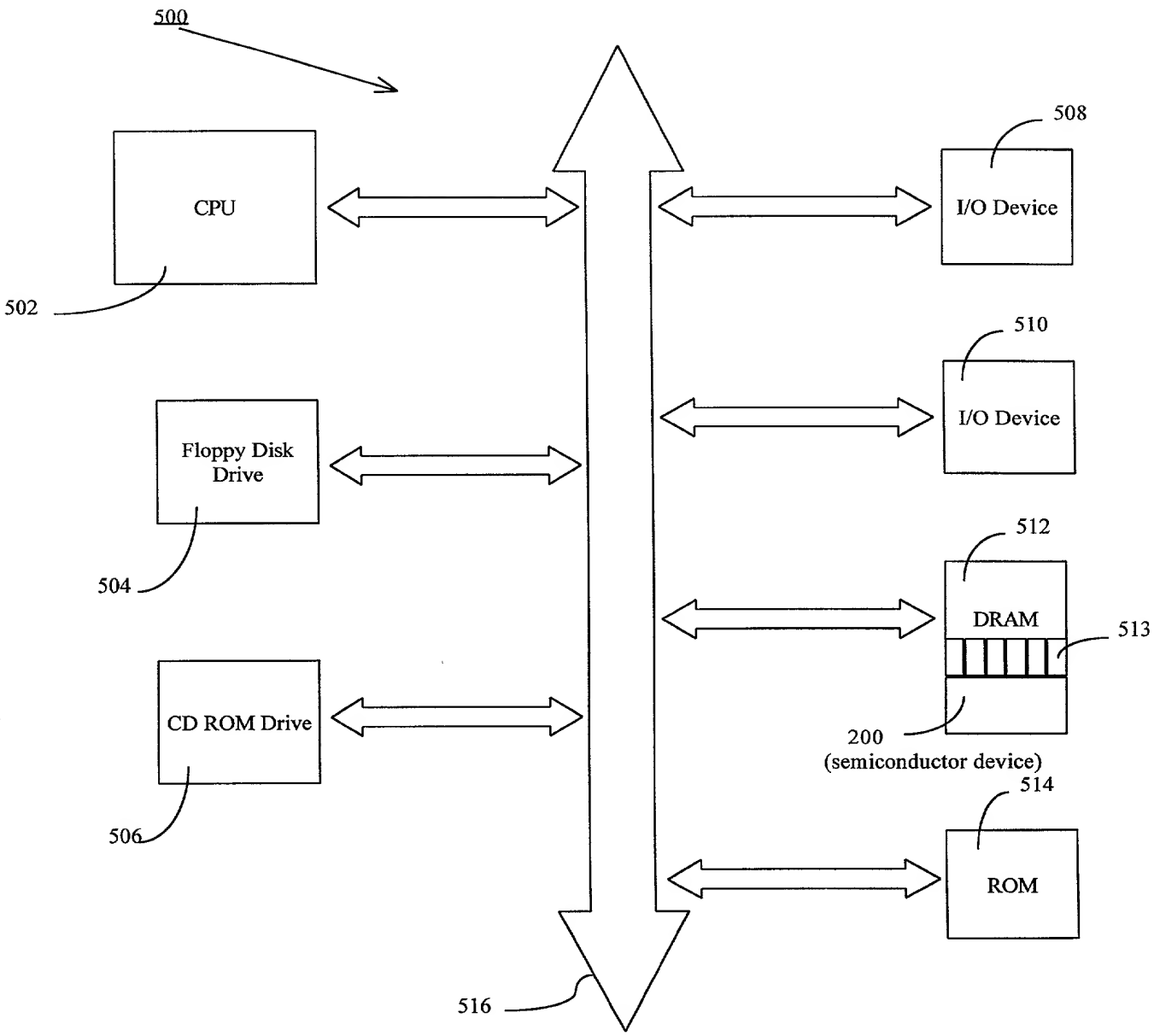

400
Deposit insulator and hard mask on substrate
405
Form opening in insulator and hard mask
410
Form conductive plug
415
Deposit BPSG over plug and insulator
420
Etch via in BPSG
435
Etch second via portion
425
Deposit first conductive layer
430
Deposit second conductive layer

FIG. 8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CPU
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Floppy Disk Drive
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CD ROM Drive
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508
I/O Device
510
I/O Device
512
DRAM
513
200
(semiconductor device)
514
ROM
516

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States

application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW

Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

Full name of sole inventor: Chih-Chen Cho

Inventor's signature: Chih-Chen Cho Date: Feb. 28, 2000

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Docket No.: M4065.0223/P223
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chih-Chen Cho

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: BACKEND METALLIZATION METHOD AND DEVICE OBTAINED THEREFROM

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., Assignee of the entire right, title and interest in the above-identified application by virtue of the Assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of located at , listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Jeremy A. Cubert, 40,399; Laurence E. Fisher, 37,131; Brian A. Lemm, 43,748; Gianni Minutoli, 41,198; Edwin Oh, P-45,319; Eric Oliver, 35,307; William E. Powell III, 39,803; Paul L. Ratcliffe, P-45,290; Mark E. Strickland, 45,138 and Salvatore P. Tamburo, P-45,153, and also attorneys of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The Assignee certifies that the above-identified assignment has been reviewed and to the best of the Assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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MICRON TECHNOLOGY, INC.

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Chief Patent Counsel
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Dated: 1-28-01